JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF INFORMATICS AND INNOVATIVE SYSTEMS

DEPARTMENT OF COMPUTER SCIENCE AND SOFTWARE ENGINEERING

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR SCIENCE IN SECURITY AND FORENICS

2ND YEAR 2ND SEMESTER 2021/2022 ACADEMIC YEAR

MAIN CAMPUS

COURSE CODE: **ICB 3214**

COURSE TITLE: **DIGITAL ELECTRONICS**

EXAM VENUE: **STREAM:** **BSC COMP SECURITY**

DATE: **DECEMBER 2022** **EXAM SESSION:**

TIME: **2.00 HOURS**

INSTRUCTIONS:

1. **Answer Question One (Compulsory) and ANY other two questions**
2. **Candidates are advised not to write on the question paper**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room**

QUESTION ONE **[30 MARKS]**

(a) Explain the significance of the following to digital systems design: [4 Marks]
   i) MOSFET
   ii) S-R FF
   iii) DEMUX
   iv) SSI

(b) A two seated airplane requires that both the pilot and the navigator have their seat belts tightened, before the plane can take off. However, it is desired that in case of solo flights, (without the navigator), the state of the navigator seat belt should not have any effect on the take off. Make the truth table and obtain the simplified logic expression foe system and design it using NAND gates. [6 Marks]

(c) Verify that AND, OR and EX-OR operations are communicative and associative. [4 Marks]

(d) Briefly explain any applications areas in which Asynchronous Sequential Circuits are preferred over Synchronous Sequential Circuits. [4 Marks]

(e) Determine the binary, octal and hexadecimal equivalent of the decimal number 80.6875_{10}. [6 Marks]

(f) Minimize the logic function $Y(A,B,C,D) = \sum m(0, ,1\ 2, , ,3\ 5\ 7, , ,8\ 911,14)$. Use Karnaugh map. Draw logic circuit for the simplified function. [6 Marks]

QUESTION TWO **[20 MARKS]**

(a) Show that

$$A + B.C = (A + B).(A + C)$$ [4 marks]

(b) Using the distributive law in question 2(*a*)(*i*), express the following equation in product of sums form with four product terms, each with a sum of three variables:

$$F = H + I.\overline{J} + K.\overline{L}$$ [4 marks]

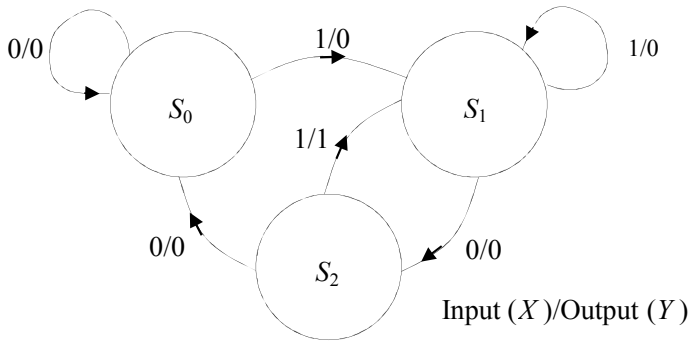
(c) A synchronous 3-bit counter implemented using D-type Flip-Flops has a mode control input *M*. When $M = 0$, the counter output sequence represented in decimal form is 0, 1, 2, 3, 4, 5, 6, 7, and repeat. When $M = 1$, the counter output sequence represented in decimal form is 0, 1, 3, 2, 6, 7, 5, 4, and repeat. The Flip-Flop outputs are $\{Z_2Z_1Z_0\}$ where Z_0 represents the least significant bit of the counter output.

   i) Draw a state diagram that describes this counter. [4 marks]
   ii) Write down the state transition table corresponding with the state diagram in question 2(*b*)(*i*). [4 Marks]
   iii) Determine the excitation combinational logic in sum of products form for D-type Flip-Flop input D_0, i.e., the input of the Flip-Flop that represents the least significant bit of the counter. Show that the required combinational logic can be implemented using a 2-input XNOR gate plus some other combinational logic gates. [4 Marks]

QUESTION THREE **[20 MARKS]**

(a) Simplify the four-variable function: $G(A,B,C,D) = \Sigma(0,2,6,7,8,9,10,13,15)$ using the Quine-McCluskey (Q-M) method. The numbers in the summation are the decimal representations of the minterms of *G* (where *A* represents the most-significant bit of the equivalent binary representation). [8 Marks]

(b) Consider the following state machine:



i) Assuming that the machine starts in state S_0 and that the input data sequence at input (X) is appropriately synchronized with the state machine clock, determine the next-state and output sequences for the input sequence 0101011011011. Also explain the operation that the machine performs. [6 marks]

ii) For an implementation based on two D-type flip-flops (labelled A and B), determine simplified Boolean expressions for the next-state and output combinational logic, assuming the state assignment $S_0 = 00$, $S_1 = 01$ and $S_2 = 10$ is used, where a state is labelled $Q_A Q_B$ in terms of the flip-flop outputs. [4 marks]

iii) Explain whether there is a feature, inherent in the proposed state-machine design, that may give rise to problems at the output Y. [2 marks]

QUESTION FOUR **[20 MARKS]**

(a) Implement the Boolean function:

$$X = A.B.C + B.C + B.C$$

using

i) an 8:1 Multiplexer [5 Marks]

ii) a 2:1 Multiplexer, plus a NOT gate, plus an OR gate [6 Marks]

(b) A *priority encoder* has 2^N inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE, or 0 if none of the inputs is TRUE. It also produces an output NONE that is TRUE if none of the inputs is TRUE.

i) Write down the Truth Table showing all inputs and all outputs for an eight-input priority encoder. [5 Marks]

ii) Give simplified Boolean expressions for all outputs of the eight-input priority encoder. [4 Marks]

QUESTION FIVE **[20 MARKS]**

(a) Compute the following:

i) Addition using 2's compliment: -20 to +26 [4 Marks]

ii) Add 648 and 487 in BCD code [4 Marks]

iii) Convert the binary number 10110_2 to Gray code [4 Marks]

(b) Using a suitable diagram, show the interfacing of two TTL gates i.e. an OR gate driving an AND gate. [4 Marks]

(c) Give *two advantages* and *two disadvantages* of CMOS ICs over TTL devices. [4 Marks]

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