JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL INFORMATICS AND INNOVATIVE SYSTEMS

UNIVERSITY EXAMINATION FOR THE DEGREE OF SCIENCE

COMPUTER SECURITY & FORENSICS

2ND YEAR 2ND SEMESTER 2013/2014 ACADEMIC YEAR

CENTRE: KISUMU

COURSE CODE: IIT 3123

COURSE TITLE: COMPUTER SYSTEM ARCHITECTURE

EXAM VENUE: **STREAM: BSc. Computer Security & Forensics**

DATE: 2/12/2013 **EXAM SESSION: 2.00 – 4.00 PM**

TIME: 2 HOURS

Instructions:

1. **Answer question 1 (Compulsory) and ANY other 2 questions.**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE

a) State any two ways of reducing external fragmentation in memory management (2 marks)
b) State the five Key tasks performed by an operating system in file management . (5 marks)
c) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number (6 marks)

d) Obtain the simplified expressions in sum of products for the following Boolean functions:
(i) $F(A,B,C,D,E) = \Sigma(0,1,4,5,16,17,21,25,29)$ (4 marks)
(ii) $A'B'CE' + A'B'C'D' + B'D'E' + B'C\,D'$ (3 marks)
e) Assuming that you are trying to fetch the instruction at memory location 2005 in an 8085 processor. That means that the Program Counter is set to that value; identify the sequence of operations. (5 marks)
f) Draw a block diagram of a sequential circuit and explain how it works (5 marks)

QUESTION TWO

a) Perform the operation of subtractions with the following binary numbers using 2′ complement (i) 10010 - 10111 (ii) 100 -110001 (iii) 11010 -10001 (6 marks)
b) Describe the working of a five bit parallel Binary adder circuit using full adders. (8 marks)

c) Explain the following terms as used in computer architecture and organization.
i) Assembler ii) Compiler iii) Machine Interpretation. (6 marks)

QUESTION THREE

a) Negative binary numbers can be represented using the sign and magnitude method or the two's complement. Outline the underlying ideas of these two methods and explain their advantages and disadvantages. (6 marks)
b) Discuss the phases of Instruction Cycle with flowchart. (8 marks)
a) Design a combinational circuit whose input is four bit binary number and output is the 2's complement of the input binary number. (6 marks)

QUESTION FOUR

a) Briefly explain the differences between RISC and CISC computer (6 marks)

b) Program counter is a register within the CPU; briefly state its core functions. (3 marks)

c) What do you understand by single-user contiguous scheme in memory management (3 marks)

d) State two disadvantages of single-user contiguous scheme (2 marks)

e) The Von Neumann architecture presents a logical view of a computer that still forms the basis of most computers as we know them today. Explain what the von Neumann architecture is and, with the help of an example, explain how it processes data. (6 marks)

QUESTION FIVE

a) Differentiate between Assembly language and Machine code language. (4 marks)

b) How can the instruction execution speed of CPU be increased? (3 marks)

c) Briefly explain the Instruction Cycle, use a flowchart diagram (4 marks)

d) Differentiate between static RAM and dynamic RAM (5 marks)

e) Apart from internal data transfer between computer components, the computer may have to communicate with its peripherals. Explain how this process is managed (4 marks)