JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL INFORMATICS AND INNOVATIVE SYSTEMS

UNIVERSITY EXAMINATION FOR THE DEGREE OF SCIENCE

COMPUTER SECURITY & FORENSICS

1ST YEAR 2ND SEMESTER 2013/2014 ACADEMIC YEAR

CENTRE: MAIN

COURSE CODE: IIT 3123

COURSE TITLE: COMPUTER SYSTEMS ARCHITECTURE

EXAM VENUE: LR 2 **STREAM: BSc. Computer Security & Forensics**

DATE: 10/12/2013 **EXAM SESSION: 11.30 – 1.30 PM**

TIME: 2 HOURS

Instructions:

1. **Answer question 1 (Compulsory) and ANY other 2 questions.**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE (30) COMPULSORY

a) Briefly define Cache Memory and explain how it may alleviate the Von Neumann bottleneck. (5 marks)
b) Discuss the phases of Instruction Cycle with flowchart. (8 marks)
c) Apart from internal data transfer between computer components, the computer may have to communicate with its peripherals. Explain how this process is managed. (4 marks)

d) Obtain the simplified expressions in sum of products for the following Boolean functions:
(i) $F(A,B,C,D,E) = \Sigma(0,1,4,5,16,17,21,25,29)$ (4 marks)
(ii) A′B′CE′ + A′B′C′D′ +B′D′E′ + B′C D′ (3 marks)
e) Perform the operation of subtractions with the following binary numbers using 2′ complement
(i) 10010 - 10011 (ii) 100 -110000 (iii) 11010 -10000 (6 marks)

QUESTION TWO (20)

a) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number. (6 marks)

b) Draw and explain a process state diagram showing the possible interactions between each of the states. (6 marks)
c) Briefly define the following terms: i) Process ii) Scheduling iii) Virtual memory iv) program counter (8 marks)

QUESTION THREE (20)
a) Describe the working of a five bit parallel Binary adder circuit using full adders. (8 marks)
b) Compute the following using 2's complement arithmetic (i) – 9 – 4 (ii) – 4 + 9 (8 marks)
c) Differentiate between Assembly language and Machine code language (4 marks)

QUESTION FOUR (20)

a) The Von Neumann architecture presents a logical view of a computer that still forms the basis of most computers as we know them today. Explain what the von Neumann architecture is and, with the help of an example, explain how it processes data. (5 marks)
b) Negative binary numbers can be represented using the sign and magnitude method or the two's complement. Outline the underlying ideas of these two methods and explain their advantages and disadvantages. (6 marks)

c) Key to multiprogramming is scheduling. Different CPU scheduling algorithms have different properties. Outline the scheduling process and describe three different scheduling methods. (9 marks)

QUESTION FIVE (20)

a) Differentiate between static RAM and dynamic RAM. (6 marks)

b) Briefly explain the differences between RISC and CISC computer. (6 marks)

c) Design a MOD 5 Synchronous Counter using D Flip Flops. (8 marks)