JARAMOGI OGINGA ODINGA UNIVERSITY OF SCENCE AND TECHNOLOGY

SCHOOL OF INFRMATICS AND INNOVATIVE SYSTEMS

COURSE CODE: IIT3226

COURSE TITLE: DIGITAL ELECTRONICS

EXAMINATIONS 2012/2013

TIME 2HRS **KLC**

INSTRUCTIONS:

i. **This paper contains five (5) questions.**
ii. **Question ONE is Compulsory and any other TWO questions**
iii. **Answer the questions on the booklet provided**
iv. **Mobile Phones are not allowed in exams room**

QUESTION ONE (30 Marks)- Compulsory

a) Simplify the following Boolean expressions using De Morgan's theorem and/ or Boolean algebra

i) $ABC + \bar{A}CD + \bar{B}CD$ (4 Marks)

ii) $AB + (C + \bar{B})(AB + \bar{C})$ (4 Marks)

b) Simplify the following Boolean equation using Karnaugh map.

F(X,Y,Z) = Σ (1,3,4,5,6) (4 Marks)

c) Express the Boolean function depicted in the K-Map shown below as Boolean equation in Product- of- Sum form (4 Marks)

AB \ CD				
	1	1	0	1
	0	1	0	0
	0	0	0	0
	1	1	0	1

d) Compare Analog and Digital systems. Explain the advantages and disadvantages of digital systems over analog systems. (6 Marks)

e) Explain the working of JK Flip Flop with the help of its logic diagram, characteristic equation, state table and excitation table. (8 Marks)

QUESTION TWO (20 Marks)

a) Draw and explain the logic circuit and truth table for an Octal to Binary Encoder (6 Marks)

b) Perform the operation of subtractions with the following binary numbers using 2′ complement

(i) 10010 - 10011 (ii) 100 -110000 (iii) 11010 -10000 (6 Marks)

c) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number. (5 Marks)

d) Demonstrate by means of truth table the validity of the De Morgan's theorems for three variables of Boolean algebra (3 Marks)

QUESTION THREE (20 Marks)

a) Implement a full adder circuit using NAND gates only, show the truth table (7 Marks)

b) With neat sketch explain the operation of clocked RS flip (7 Marks)

c) Perform the following decimal arithmetic calculations by first converting the given decimal numbers into their binary equivalent then using 2's complement effect the calculation. (6 Marks)

i) 48- 72

ii) 524- 320

QUESTION FOUR (20 Marks)

a) Describe the architecture of PALs with the aid of one or more illustrative diagrams. (4 Marks)

b) Indicate clearly how a PAL device would be programmed to implement a full adder (4 Marks)

c) Design a 3-to- 8 decoder (8 Marks)

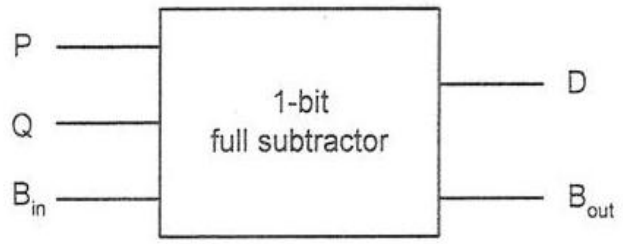
a) Implement Boolean expression for Ex-OR gate using NAND gates only (4Marks)

QUESTION FIVE (20 Marks)

a) The 1-bit full Subtractor shown below performs the binary subtraction ($P-Q-B_{in}$) where P and Q are 1 –bit variables and B_{in} is a borrow input from the previous stage. It produces two outputs: the difference D and the borrow output B_{out}. The truth table describing the function of the 1-bit full Subtractor is also shown.

i) Derive the Boolean equations for D and B_{out} (3 Marks)

ii) Implement these equations using only NOR gates (5 Marks)



B_{in}	P	Q	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

b) Draw and explain the logic circuit and truth table for an Octal to Binary Encoder. (6 Marks)

c) Give classification of counters and explain any one of them (6 Marks)