JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF BIOLOGICAL AND PHYSICAL SCIENCES

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR OF EDUCATION

SCIENCE WITH IT

2022/2023 ACADEMIC YEAR   4th YEAR   1ST SEMESTER

MAIN

REGULAR

COURSE CODE: SPB 9429

COURSE TITLE: DIGITAL ELECTRONICS II

EXAM VENUE: STREAM: (BED SCI.)

DATE: EXAM SESSION:

TIME: 2 HOURS

Instructions:

1. **Answer question 1 (compulsory) and ANY other 2 questions.**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE

a. Define a sequential logic circuit and give an example of one.   (3 marks)

b. Draw the truth table of a full subtractor circuit hence write down the logic function of the Difference and Borrow in outputs   (4 marks)

c. Draw the schematic block diagram of a 4-bit multiplier   (3 marks)

d. Define a magnitude comparator   (2 marks)

e. Differentiate between;

   i) synchronous and asynchronous inputs;

ii) level-triggered and edge-triggered flip-flops   (4 marks)

f. A series counter has a modulus of 32,768. If all the flip flops used to construct the counter are identical and each has a propagation delay of 0.02 seconds. Determine the propagation   delay   of   the   counter
(3 marks)

g. Briefly describe the following flip-flop timing parameters:
   i)   set-up time and hold time;
   ii)   propagation delay;
   iii)   maximum clock frequency.   (4 marks)

h. i)   What is meant by the 'race problem' in flip-flops?   (2 marks)
   ii)   Explain how a master–slave flip flop configuration helps in solving this problem
                                                                (3 marks)

i. Explain why Shift registers are mainly made of D-type flip flops.   (2 marks)

SECTION B

QUESTION TWO

a.   Using well illustrated logic circuit diagrams, explain the operations of the following flip flops.
   i)   basic R-S flip-flop having active LOW inputs, (include its truth table). (8 marks)
   ii)   Clocked J-K flip-flop   (6 marks)
   iii)   Master- Slave flip flop (address the race-problem solution)   (6marks)

QUESTION THREE

a. Construct the truth table of a full subtractor circuit and from the table write down the Boolean expressions for the Difference and Borrow out outputs   (4 marks)

b. Obtain the simplified versions of the Boolean expressions obtained in (a) above hence draw the hardware of the full subtractor circuit.   (6 marks)

c. Design a 16-to-1 multiplexer using two 8-to-1 multiplexers having an active LOW ENABLE input. Fully explain the working mechanism of your design   (10 marks)

QUESTION FOUR

a. Outline any three differences between a ripple counter and a parallel counter.   (3 marks)
b. Design a 4-bit asynchronous counter and fully explain its working mechanism showing the timing waveforms sourced at the output of each flip flop.   (7 marks)
c. Briefly explain the operation of the following counters
   i)   Decade counter   (5 marks)
   ii)   BCD counter   (5 marks)

QUESTION FIVE
a. Define a shift register.   (2 marks)

b. Briefly describe the following types of shift registers citing their unique features that make them perform their tasks

   i)   Universal shift register   (3 marks)

   ii)   Bidirectional shift register   (3 marks)

c. Using well illustrated circuit diagrams, fully explain the operation of the following types of shift registers

   i)   Serial-In Serial Out shift registers   (6 marks)

   ii)   Serial-In parallel Out shift registers   (6 marks)