JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF BIOLOGICAL AND PHYSICAL SCIENCES

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR OF EDUCATION SCIENCE WITH IT

4TH YEAR 1ST SEMESTER 2018/2019 ACADEMIC YEAR

MAIN CAMPUS

COURSE CODE: SPH 406

COURSE TITLE: DIGITAL ELECTRONICS II

EXAM VENUE: **STREAM: (BED SCI.)**

DATE: **EXAM SESSION:**

TIME: 2 HOURS

Instructions:

1. **Answer question 1 (compulsory) and ANY other 2 questions.**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE

a. Distinguish between combinational and sequential logic circuits. Draw the basic block circuit diagram of each. (4 marks)

b. Distinguish between half adder and full adder circuits (2 marks)

c. Draw the truth table of a full adder circuit (3 marks)

d. What is a flip-flop (2 marks)

e. Differentiate between;

i) synchronous and asynchronous inputs;

ii) level-triggered and edge-triggered flip-flops; (4 marks)

f. Define the modulus of a counter (2 marks)

g. Briefly describe the following flip-flop timing parameters:

i) set-up time and hold time;

ii) propagation delay;

iii) maximum clock frequency. (4 marks)

h. i) What is meant by the 'race problem' in flip-flops? (2 marks)

ii) Explain how a master–slave flip flop configuration helps in solving this problem (3 marks)

i. Distinguish between synchronous and asynchronous counters (4 marks)

SECTION B

QUESTION TWO

a. i. Fully explain the logic operation of an R-S flip-flop having active LOW inputs. Draw its logic implementation and truth table. (8 marks)

b. With aid of a logic circuit diagram explain the operation of a clocked J-K flip-flop (6 marks)

c. With the help of the logic diagram fully explain the operation of a master- slave flip flop. (6marks)

QUESTION THREE

a. i) Construct the truth table of a full adder circuit and from the table write down the Boolean expressions for the Sum and Carry outputs (5 marks)

ii) Obtain the simplified versions of the Boolean expressions obtained in (a) above hence draw the hardware of the full adder circuit (5 marks)

b. i) Construct the truth table of a full subtractor circuit and from the table write down the Boolean expressions for the Difference and Borrow out outputs (5 marks)

ii) Obtain the simplified versions of the Boolean expressions obtained in (b) above hence draw the hardware of the full subtractor circuit (5 marks)

QUESTION FOUR

a. i) Draw a well labelled Hardware implementation of a four-bit ripple counter. (3 marks)

ii) Fully explain the operation basics of the counter implemented above (5 marks)

iii) Show the waveforms appearing at the outputs as the clock signal goes through successive cycles of trigger pulses. (2 marks)

b. i) Draw a well labelled Hardware implementation of a four-bit synchronous counter. (3 marks)

ii) Fully explain the operation basics of the four-bit synchronous counter implemented above (5 marks)

iii) Show the waveforms appearing at the outputs as the clock signal goes through successive cycles of trigger pulses. (2 marks)

QUESTION FIVE

a. By drawing schematic logic architecture and timing waveforms, fully explain the working operations of :

i. Serial-In Serial Out shift registers

ii. Serial-In Serial Out shift registers

iii. Serial-In Serial Out shift registers

iv. Serial-In Serial Out shift registers (20 marks)