JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF INFORMATICS AND INNOVATIVE SYSTEMS

DEPARTMENT OF INFORMATION SYSTEMS AND TECHNOLOGY

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR OF COMPUTER SECURITY & FORENSIC

1st YEAR 2nd SEMESTER 2024/2025 ACADEMIC YEAR

MAIN CAMPUS

COURSE CODE: ICB 1104

COURSE TITLE: COMPUTER SYSTEMS ARCHITECTURES

EXAM VENUE: STREAM: BSC COMPUTER SECURITY & FORENSIC

DATE: 25/4/2025 EXAM SESSION: 15.00-17.00
TIME: 2.00 HOURS

INSTRUCTIONS:

1. **Answer Question 1 (Compulsory) and ANY other two questions.**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE (30 MKS)

a) Discuss the **FOUR** functions frequently executed by computing systems. (4 mks)

b) A computer should have a set of instructions that allows the user to formulate any data processing task. Discuss the following instruction types as used in this respect:
   i) Data processing (2 mks)
   ii) Data storage (2 mks)
   iii) Data movement (2 mks)
   iv) Control (2 mks)

c) A system bus consists, typically, of from about 50 to hundreds of separate lines. Each line is assigned a particular meaning or function. Discuss the function of the following system buses:
   i) Data bus (3 mks)
   ii) Control bus (3 mks)
   iii) Address bus (3 mks)

d) A pipeline hazard occurs when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution. Explain the following hazards:
   i) Resource hazards (4 mks)
   ii) Data hazards (5 mks)

QUESTION TWO (20 MKS)

While the chipmakers have been busy learning how to fabricate chips of greater and greater density, the processor designers must come up with ever more elaborate techniques for improved performance. Discuss the following techniques built into contemporary processors to achieve this objective:

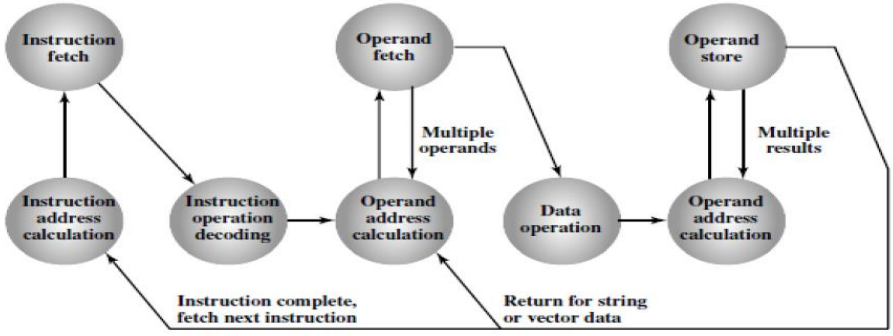
i) Branch prediction (7 mks)

ii) Data flow analysis (6 mks)

iii) Speculative execution (7 mks)

QUESTION THREE (20 MKS)

The following diagram shows a typical *instruction cycle state diagram*. Study it carefully and use it to answer the questions that follow.

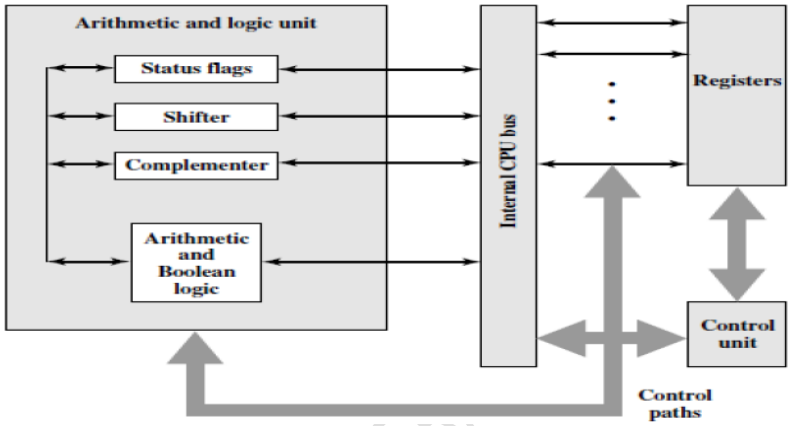


Using appropriate examples, discuss the following elements of the instruction cycle above.

a) Operation code (5 mks)
b) Source operand reference (5 mks)
c) Result operand reference (5 mks)
d) Next instruction reference (5 mks)

QUESTION FOUR (20 MKS)

The diagram below illustrates the internal structure of the central processing unit (CPU). Study it keenly and use it to answer the questions that follow.



Describe the roles played by the following components in the above structure.

i) Internal CPU bus (5 mks)
ii) Registers (5 mks)
iii) Arithmetic and logic unit (5 mks)
iv) Control unit (5 mks)

QUESTION FIVE (20 MKS)

Traditionally, the dominant factor in computing systems' performance gains has been in increases in clock speed due and logic density. However, as clock speed and logic density increase, a number of obstacles become more significant. Discuss the following issues as utilized in this respect.

i) Power (7 mks)

ii) RC delay (6 mks)

iii) Memory latency (7 mks)