JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF INFORMATICS AND INNOVATION SYSTEMS

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE

COMPUTER SECURITY AND FORENSIC

2ND YEAR 2ND SEMESTER 2013/2014 ACADEMIC YEAR

MAIN

COURSE CODE: IIT 3226

COURSE TITLE: DIGITAL ELECTRONICS

EXAM VENUE: CL I **STREAM: (BSc. Computer Security and Forensic)**

DATE: 16/04/14 **EXAM SESSION: 2.00 – 4.00 PM**

TIME: 2.00 HOURS

Instructions:

1. **Answer question 1 (Compulsory) and ANY other 2 questions**
2. **Candidates are advised not to write on the question paper.**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room.**

QUESTION ONE (30 Marks)- Compulsory

a) Demonstrate by means of truth table the validity of the De Morgan's theorems for three variables of Boolean algebra (4 Marks)

b) Simplify the following Boolean expressions using De Morgan's theorem and/ or Boolean algebra

i) $ABC + \bar{A}CD + \bar{B}CD$ (4 Marks)

ii) $AB + (C + \bar{B})(AB + \bar{C})$ (4 Marks)

c) Give classification of counters and explain any one of them (6 Marks)
Counters are circuits that cycle through a specified number of states.

d) Express the Boolean function depicted in the K-Map shown below as Boolean equation in Product-of- Sum form (4 Marks)

AB \ CD				
	1	1	0	1
	0	1	0	0
	0	0	0	0
	1	1	0	1

e) Explain the working of JK Flip Flop with the help of its logic diagram, characteristic equation, state table and excitation table. (8 Marks)

QUESTION TWO (20 Marks)

a) Draw and explain the logic circuit and truth table for an Octal to Binary Encoder (6 Marks)

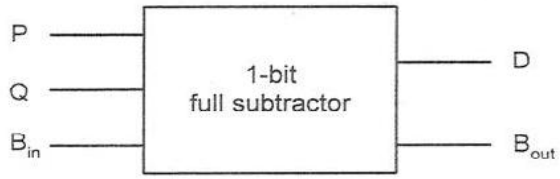
b) Perform the operation of subtractions with the following binary numbers using 2′ complement

(i) 10010 - 10011

(ii) 100 -110000

(iii) 11010 -10000 (6 Marks)

c) The 1-bit full Subtractor shown below performs the binary subtraction ($P-Q-B_{in}$) where P and Q are 1 –bit variables and B_{in} is a borrow input from the previous stage. It produces two outputs: the difference D and the borrow output B_{out}. The truth table describing the function of the 1-bit full Subtractor is also shown.



B_{in}	P	Q	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

i) Derive the Boolean equations for D and B_{out} (3 Marks)

ii) Implement these equations using only NOR gates (5 Marks)

QUESTION THREE (20 Marks)

a) Implement a full adder circuit using NAND gates only, show the truth table (7 Marks)

b) With neat sketch explain the operation of clocked RS flip (7 Marks)

c) Perform the following decimal arithmetic calculations by first converting the given decimal numbers into their binary equivalent then using 2's complement effect the calculation. (6 Marks)

i) 48- 72 ii) 524- 320

QUESTION FOUR (20 Marks)

a) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number. (5 Marks)
b) Describe the architecture of PALs with the aid of one or more illustrative diagrams. (4 Marks)
c) Design a 3-to- 8 decoder (8 Marks)
d) Briefly explain the problem of SR Flip Flop and state what measures you can take to eliminate or solve it (3 Marks)

QUESTION FIVE (20 Marks)

a) Indicate clearly how a PAL device would be programmed to implement a full adder (4 Marks)
b) Compare Analog and Digital systems. Explain the advantages and disadvantages of digital systems over analog systems. (6 Marks)
c) Implement Boolean expression for Ex-OR gate using NAND gates only (4Marks)
d) Describe the working of a five bit parallel Binary adder circuit using full adders. (6 Marks)