JARAMOGI OGINGA ODINGA UNIVERSITY OF SCIENCE AND TECHNOLOGY

SCHOOL OF INFORMATICS AND INNOVATIVE SYSTEMS

UNIVERSITY EXAMINATION FOR THE DEGREE OF BACHELOR SCIENCE IN COMPUTER SECURITY AND FORENSIC

2ND YEAR 2ND SEMESTER 2015/2016 ACADEMIC YEAR

SPECIAL/ RESIT

MAIN CAMPUS

COURSE CODE: IIT 3226

COURSE TITLE: DIGITAL ELECTRONICS

EXAM VENUE: **STREAM:**

DATE: 06/05/16 **EXAM SESSION: 9.00 – 11.00 AM**

TIME: 2.00 HOURS

INSTRUCTIONS:

1. **Answer Question 1 (Compulsory) and ANY other two questions**
2. **Candidates are advised not to write on the question paper**
3. **Candidates must hand in their answer booklets to the invigilator while in the examination room**

QUESTION ONE

a) Construct the truth tables for the following logic gates

i) AND gate **(2marks)**

ii) OR gate **(2marks)**

iii) EX-NOR gate **(2marks)**

b) Use an example to demonstrate how;

i) Hexadecimal Number can be converted to an equivalent Octal Number. **(2marks)**

ii) The same decimal number can be represented in binary form using both Natural BCD Code and Excess-3 code. **(2marks)**

e) Briefly explain two advantages associated with synchronous counters **(4marks)**

f) Distinguish between analogue and digital systems **(4marks)**

g) State two advantages and disadvantages of ring counters **(4marks)**

h) Explain what you understand by sequential and combinational logic **(4marks)**

i) State any four Boolean algebraic identities **(4marks)**

QUESTION TWO

a) Define the following terms and concepts as applies to computer aided design for digital systems **(8marks)**

i) Design entity

ii) Logic Synthesis

iii) Timing Simulation

iv) Chip Configuration

b) What is a Demultiplexer? **(2marks)**

c) Discuss the differences between a Demultiplexer and a decoder. **(4marks)**

d) Prove the following equations using the Boolean algebraic theorems: **(6 Marks)**

(i) $A + \bar{A} .B + A . \bar{B} = A + B$

(ii) $\bar{A}BC + A \bar{B} C + AB\bar{C} + ABC = AB + BC + AC$

QUESTION THREE

A combinational logic circuit takes a 4-bit unsigned binary integer number at its inputs labelled D_3, D_2, D_1 and D_0, where D_3 is the most significant bit. For decimal input 1, 2, 3, 5, 7, 11 and 13, the output S is to be at logic 1, and it is to be at logic 0 otherwise.

(a) Write down the truth table for the required combinational logic function. **(4 Marks)**

(b) Using a Karnaugh map, determine the simplified Boolean expression for the output S in terms of the inputs D_3 to D_0 in a minimum sum-of-products form. **(6 Marks)**

(c) Describe what is meant by an essential term in a Karnaugh map. Write down the essential terms for the Karnaugh map in (b). **(4 Marks)**

(d) Using a Karnaugh map, this time determine the required simplified Boolean expression for the output S in a minimum product-of-sums form. **(6 Marks)**

QUESTION FOUR

a) Define the term clock as used in digital electronics **(2marks)**

b) Construct an AND gate and an OR gate using NAND gates only **(8marks)**

c) State and prove Demorgan's laws. **(4Marks)**

d) With the help of a truth table explain the working of a half Subtractor. Draw the logic diagram using gates.. **(6Marks)**

QUESTION FIVE

a) Determine the binary numbers represented by the following decimal numbers. **(6Marks)**

i) 25.5
ii) 10.625
iii) 0.6875

b) Using a suitable example, identify and explain a logic operation which is;

i) Both Communicative and Associative **(3Marks)**

ii) Communicative but not Associative **(3Marks)**

c) Design a four bit ring counter using the simple flip flop **(4marks)**

d) Construct an AND gate and an OR gate using NAND gates only **(4 marks)**